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1. A differential amplifier for providing common-mode rejection while providing differential-mode amplification, comprising:
   a. an active differential amplification element electrically coupled to a first input signal, a second input signal and an output signal, the active differential amplification element also electrically coupled to a first voltage and a different second voltage; and
   b. a passive bias element electrically coupled to the active differential amplification element, the passive bias element capable of biasing the active differential amplification element so that the active differential amplification element operates in a saturation mode, thereby generating the output signal so that the output signal corresponds to a voltage difference between the first input signal and the second input signal.

2. (Amended) The differential amplifier of Claim 1, wherein the active differential amplification element comprises:
   a. a first transistor having a first source electrically coupled to the first voltage, a first gate electrically coupled to a first node and a first drain, the first node being a bias node;
   b. a second transistor having a second drain, a second gate electrically coupled to the first node and a second source electrically coupled to the second voltage different from the first voltage;
   c. a third transistor having a third source electrically coupled to the first voltage, a third drain and a third gate electrically coupled to the first node;
   d. a fourth transistor having a fourth drain, a fourth gate electrically coupled to the first node and a fourth source electrically coupled to the second voltage;

e. a fifth transistor having a fifth source electrically coupled to the first voltage, a fifth drain electrically coupled to a second node and a fifth gate electrically coupled to the first node;

f. a sixth transistor having a sixth drain electrically coupled to a third node, a sixth gate electrically coupled to the first node and a sixth source electrically coupled to the second voltage;

g. a seventh transistor having a seventh source electrically coupled to the second node, a seventh drain electrically coupled to the second drain, and a seventh gate electrically coupled to a first input signal;

h. an eighth transistor having an eighth drain electrically coupled to the first drain, an eighth source electrically coupled to the third node and an eighth gate electrically coupled to the first input signal;

i. a ninth transistor having a ninth source electrically coupled to the second node, a ninth gate electrically coupled to a second input signal and a ninth drain electrically coupled to the fourth drain; and

j. a tenth transistor having a tenth drain electrically coupled to the third drain, a tenth gate electrically coupled to the second input signal and a tenth source electrically coupled to the third node.

3. (Amended) The differential amplifier of Claim 2, wherein the passive bias element comprises:

a. a first resistor electrically coupling the first drain to the first node;

b. a second resistor electrically coupling the second drain to the first node;

c. a third resistor electrically coupling the third drain to the output signal; and

d. a fourth resistor electrically coupling the fourth drain to the output signal.

4. The differential amplifier of Claim 1, wherein the first transistor, the third transistor, the fifth transistor, the seventh transistor and the ninth transistor each comprise a p-channel device.

5. The differential amplifier of Claim 1, wherein the second transistor, the fourth transistor, the sixth transistor, the eighth transistor and the tenth transistor each comprise an n-channel device.

6. The differential amplifier of Claim 1, wherein the second voltage is electrically coupled to a common ground.

7. (Amended) A differential amplifier for providing common-mode rejection while providing differential-mode amplification, comprising:

a. a first transistor having a first source electrically coupled to a first voltage, a first gate electrically coupled to a first node and a first drain, the first node being a bias node;

b. a second transistor having a second drain, a second gate electrically coupled to the first node and a second source electrically coupled to a second voltage different from the first voltage;

c. a first resistor electrically coupling the first drain to the first node;

d. a second resistor electrically coupling the second drain to the first node;

e. a third transistor having a third source electrically coupled to the first voltage, a third drain and a third gate electrically coupled to the first node;

f. a fourth transistor having a fourth drain, a fourth gate electrically coupled to the first node and a fourth source electrically coupled to the second voltage;

g. a third resistor electrically coupling the third drain to an output signal;

h. a fourth resistor electrically coupling the fourth drain to the output signal;

i. a fifth transistor having a fifth source electrically coupled to the first voltage, a fifth drain electrically coupled to a second node and a fifth gate electrically coupled to the first node;

j. a sixth transistor having a sixth drain electrically coupled to a third node, a sixth gate electrically coupled to the first node and a sixth source electrically coupled to the second voltage;

k. a seventh transistor having a seventh source electrically coupled to the second node, a seventh drain electrically coupled to the second drain, and a seventh gate electrically coupled to a first input signal;

l. an eighth transistor having an eighth drain electrically coupled to the first drain, and an eighth source electrically coupled to the third node and an eighth gate electrically coupled to the first input signal;

m. a ninth transistor having a ninth source electrically coupled to the second node, a ninth gate electrically coupled to a second input signal and a ninth drain electrically coupled to the fourth drain; and

n. a tenth transistor having a tenth drain electrically coupled to the third drain, a tenth gate electrically coupled to the second input signal and a tenth source electrically coupled to the third node.

8. The differential amplifier of Claim 7, wherein the first transistor, the third transistor, the fifth transistor, the seventh transistor and the ninth transistor each comprise a p-channel device.

9. The differential amplifier of Claim 7, wherein the second transistor, the fourth transistor, the sixth transistor, the eighth transistor and the tenth transistor each comprise an n-channel device.

10. The differential amplifier of Claim 7, wherein the second voltage is electrically coupled to a common ground.